REMARKS / DISCUSSION OF ISSUES

The present amendment is submitted in response to the Final Office Action mailed May 13, 2009. In view of the remarks to follow, reconsideration and allowance of this application are respectfully requested.

Status of the Claims

Claims 1-15 remain in this application. Claims 1-10 have been indicated as being allowable. Claims 11 and 13 have been amended.

Allowable Subject Matter

Applicants wish to thank the Examiner for indicating that Claims 1-10 are allowable.

Rejections under 112, Second Paragraph

In the Office Action, claim 13 was rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as his invention. Claim 13 has been amended in a manner which is believed to overcome the rejection. Specifically, Claim 13 has been amended to remove the objectionable recitation "the channel" making the claim indefinite.

Rejections under 35 U.S.C. §102(e)

I. Claims 11-15 are allowable

In the Office Action, Claims 11-15 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Application No. 2004/0088637 ("Wada"). Applicants respectfully traverse the rejections.

The cited portions of Wada do not anticipate claim 11, because the cited portions of Wada fail to disclose every element of claim 11, as more precisely and specifically claimed. For example, the cited portions of Wada fail to disclose or suggest, "*wherein said slicer apparatus performs threshold decisions in respect of said received high frequency signal waveform, and performs adjustments of the slicer-level in accordance with said threshold decisions based on calculating a running digital sum (RDS) signal that is used in the DC-*

control bits generation in encoding.", as recited in claim 11. It is respectfully submitted that a careful examination of the cited portions of Wada, see par. 29, and specifically slicer 13 thereof, will show that the above recitation of claim 11 is not clearly met.

Applicants respectfully submit that the slicer apparatus taught in Wada and the invention include similarities and differences. In one aspect, the slicers are similar in that they are both configured to set a threshold based on a binarized input signal. However, in a further aspect, the slicers are dissimilar in that, with regard to the slicer of the instant invention, on the receiver side, the slicer determination is based on calculating a running digital sum (RDS) signal that is used in the DC-control bits generation in encoding, as more precisely and specifically claimed in claim 11. That is, the slicer in the receiver sets its position at which an RDS signal gets minimized. The RDS is calculated using the threshold decisions at the output signal of the slicer.

The Office asserts, at pages 2-3 of the Office Action, that Wada discloses a receiver with a slicer apparatus for controlling the DC-level of a received high frequency signal waveform, wherein said slicer apparatus performs threshold decisions in respect of said received high frequency signal waveform and performs adjustments of the slicer-level in accordance with said threshold decisions. Applicants acknowledge that adjustments of the slicer-level are taught in both the instant invention and Wada, however, a key difference between Wada and the instant invention is the manner in which the adjustments are performed. More particularly, the slicer in Wada may be differentiated from the slicer of the instant invention in that the slicer in Wada **does not** make its determination based on calculating a running digital sum (RDS) signal that is used in the DC-control bits generation in encoding, as more precisely and specifically claimed in claim 11.

In contrast to the instant invention, Wada teaches that the threshold value is adjusted by setting an optimal DC position by minimizing a bit error rate calculated after a bit detector. See Wada, par. 29:

[0029] ...a slice balance adjustment circuit 18 connected to error rate detection circuit 16 and slicer 13 for adjusting a threshold value in binarization by slicer 13 to reduce an error rate in error rate detection circuit 16, ...

A pre-requisite of Wada is that the receiver is able to find a particular location on the disc where the bits reside that are a-priori known, in terms of '0' or '1', in order to calculate a bit error rate. In contrast to Wada, and discussed above, the slicer position, according to the instant invention, is determined by minimizing a running digital sum (RDS) signal that is calculated only using the immediate output of the slicer without the need to have any known bits on the disc, as required by Wada. In this manner, the instant invention provides a receiver for an optical data storage system optical data storage system, arranged to enable the slicer control to be performed at a faster rate relative to prior art arrangements that use simple threshold bit-decisions on the signal waveform.

Based on the foregoing, it is respectfully submitted that claim 11 is allowable.

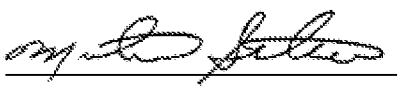
Claims 12-15 depend from claim 11, which Applicant has shown to be allowable. Hence the cited portions of Wada fail to disclose or suggest at least one element of each of claims 12-15. Accordingly, claims 12-15 are also allowable, at least by virtue of their dependence from claim 11.

Conclusion

In view of the foregoing amendments and remarks, it is respectfully submitted that all claims presently pending in the application, namely, Claims 1-15 are believed to be in condition for allowance and patentably distinguishable over the art of record.

If the Examiner should have any questions concerning this communication or feels that an interview would be helpful, the Examiner is requested to call Mike Belk, Esq., Intellectual Property Counsel, Philips Electronics North America, at 914-945-6000.

Respectfully submitted,



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